IBM

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings of claims in the application.

**LISTING OF CLAIMS:**

What is claimed is:

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)
15. (Cancelled)
16. (Cancelled)
17. (Currently Amended) A device for parameter independent buffer underrun prevention in a data communication system comprising a buffer for compensating for a difference in the rate of flow of data having an write port for writing data into said buffer and a read port for reading data from said buffer, said device comprising:

a memory unit for storing a predetermined delay time,

a counter for measuring said predetermined delay time,



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a signal generator for generating a signal enabling read access to said buffer after said delay time has passed,

means for determining the length of a time gap between the completion of writing data into said buffer and completion of reading data from said buffer,

a computing unit for decreasing the length of said predetermined delay time by a first value if the length of said time gap is larger than a specified tolerance value, and

wherein said computing unit increases the length of said predetermined delay time by a second value if the length of said time gap is smaller than said specified tolerance value.

further comprising means for storing the decreased or increased length of said predetermined delay in said memory unit, and

wherein in said data communication system data packets of varying size are written into and read from said buffer and said data packets are classified according to their size into different packet classes, the device further comprising a first input port for receiving a class signal specifying said particular packet class and additional memory units for storing a designated predetermined delay time for each packet class,

and further comprising a second input port for receiving an end-of-read signal signaling the instant of time when only a specified number of cycles are left before all data are read from said buffer,



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and further comprising a third input port for receiving a write signal signaling when data are written into said buffer, and

~~The device according to claim 16,~~ wherein said means for determining the length of said time gap between the completion of writing data into said buffer and completion of reading data from said buffer is formed by a logical unit determining whether or not said end-of-read signal occurs while said write signal is still signaling that data are written into said buffer.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)



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